REMARKS

In response to the Office Action mailed January 31, 2007, and in view of the Request for Continued Examination (RCE) filed concurrently herewith, Applicants respectfully request reconsideration. Claims 1-32 were previously pending in this application. Claims 1, 10, 13, 30 and 32 have been amended herein. New claims 33-36 have been added to more fully define Applicants' contribution to the art. As a result, claims 1-36 are pending for examination with claims 1 and 13 being independent. No new matter has been added.

Objections to the Claims

The Office Action objected to claim 10, stating that it was not understood how a voltage-regulator circuit associated to the first load is used for maintaining the first conduction terminal of the second load at a pre-set voltage. In response, applicants have amended claim 10 to recite a voltage-regulator circuit associated with said first load for maintaining said first conduction terminal of said first load at a pre-set voltage. Accordingly, withdrawal of this objection is respectfully requested.

Rejections Under 35 U.S.C. §103

The Office Action rejected independent claims 1 and 13 under 35 U.S.C. 103(a) as being purportedly unpatentable over Pollachek, 4,648,074, in view of Lee et al., 5,909,405. Applicants respectfully request reconsideration.

The Office Action relies primarily on the Pollachek reference in rejecting the claims of the present application. FIG. 3 of Pollachek illustrates a memory in which a bit line and a reference line are precharged to a voltage V_{DD} prior to reading the contents of a memory stack. To apply the precharge voltage to the reference line, transistor PTR is turned on momentarily so that the voltage V_{DD} is transferred to the reference line (col. 5, lines 52-56). Once the precharge stage is completed, transistor PTR is turned off. Then, reference circuit select transistor T_R is turned on so that the data stored in the cell can be read by differential sense amplifier 22 based on the respective voltages V_S and V_R provided by the reference and memory cells (Col. 5, lines 14-37 and 52-56). Pollachek does not teach or suggest that transistor PTR provides a current to the reference cells because transistor T_R is not turned on at the same time as transistor PTR (Col. 5, lines 52-56). Rather, the current provided from transistor PTR is used to charge capacitor C2.

The charge stored in capacitor C2 is later used for a differential read-out based on the resulting memory cell and reference cell voltages (Col. 5, lines 14-37 and 52-56).

Pollacheck does not describe the circuit that is used for providing precharge pulses PC to precharge transistors PT1 and PTR. However, it should be clear from Pollacheck (FIG. 3) that the precharge pulses PC received by transistors PT1 and PTR are not provided by one of the conduction terminals of transistors PT1 and PTR, but rather are provided by a different circuit (not shown).

By contrast, claim 1 as amended recites, *inter alia*, a sense amplifier for nonvolatile memory cells comprising .... a control circuit controlling said first load .... wherein the first load is controlled by the control circuit in response to a voltage of the first conduction terminal of the first load. Pollachek does not teach or suggest a load that is controlled by a control circuit in response to a voltage of a conduction terminal of the load. Lee fails to remedy this deficiency of Pollachek. Therefore, claim 1 patentably distinguishes over the combination of Pollachek and Lee proposed in the Office Action. Accordingly, withdrawal of this rejection is respectfully requested.

Claims 2-12 depend from claim 1 and are therefore patentable for at least the same reasons.

Claim 13 as amended recites, *inter alia*, a sense amplifier for a memory cell, comprising .... a control circuit coupled to a control input of the first transistor and the first conducting terminal of the first transistor such that the control circuit applies a control voltage to the control input of the first transistor in response to a voltage of the first conducting terminal. Pollachek does not teach or suggest applying a control voltage to the control input of a transistor in response to a voltage of a conducting terminal of the transistor. Lee fails to remedy this deficiency of Pollachek. Therefore, claim 13 patentably distinguishes over the combination of Pollachek and Lee proposed in the Office Action. Accordingly, withdrawal of this rejection is respectfully requested.

Claims 14-36 depend from claim 13 and are therefore patentable for at least the same reasons.

CONCLUSION

A Notice of Allowance is respectfully requested. The Examiner is requested to call the undersigned at the telephone number listed below if this communication does not place the case in condition for allowance.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

Dated: July 2, 2007

Respectfully submitted,

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